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V. Vannall

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/420,635
Filing Date ..... October 21, 1999
Inventor ..... Werner Juengling
Assignee ..... Micron Technology, Inc.
Group Art Unit 2812
Examiner ..... H. Tsai
Attorney's Docket No. MI22-1243
Title: Semiconductor Processing Methods of Forming Devices on a Substrate, Forming Device Arrays on a Substrate, Forming Conductive Lines on a Substrate, and Forming Capacitor Arrays on a Substrate, and Integrated Circuitry

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents listed on the attached Form PTO-1449. No admission is made regarding whether the submitted references are prior art.

Further, Applicant herewith submits a Supplemental Information Disclosure Statement and Form PTO-1449 of which it does not yet have an initialed copy from the Examiner. This Information Disclosure Statement was initially submitted to the U.S. Patent and Trademark Office on January 25, 2001. To the extent the PTO-1449 has not already been initialed in the file, such examination and initialing is requested at this time, and returning of a copy to the undersigned.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: May 9, 2001

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